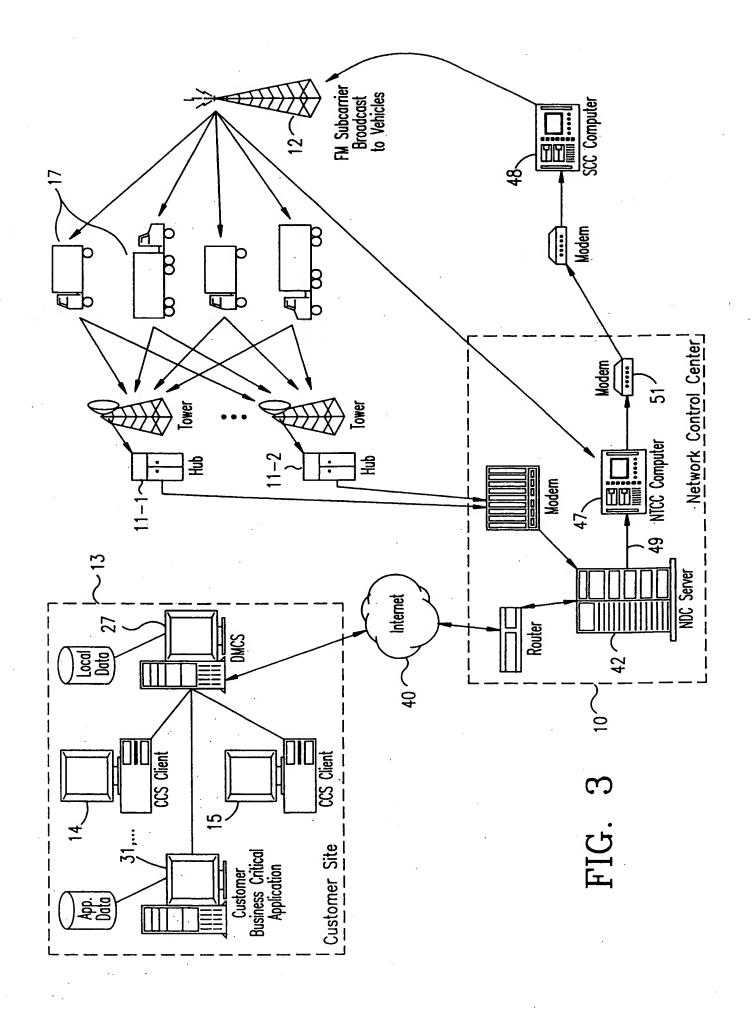
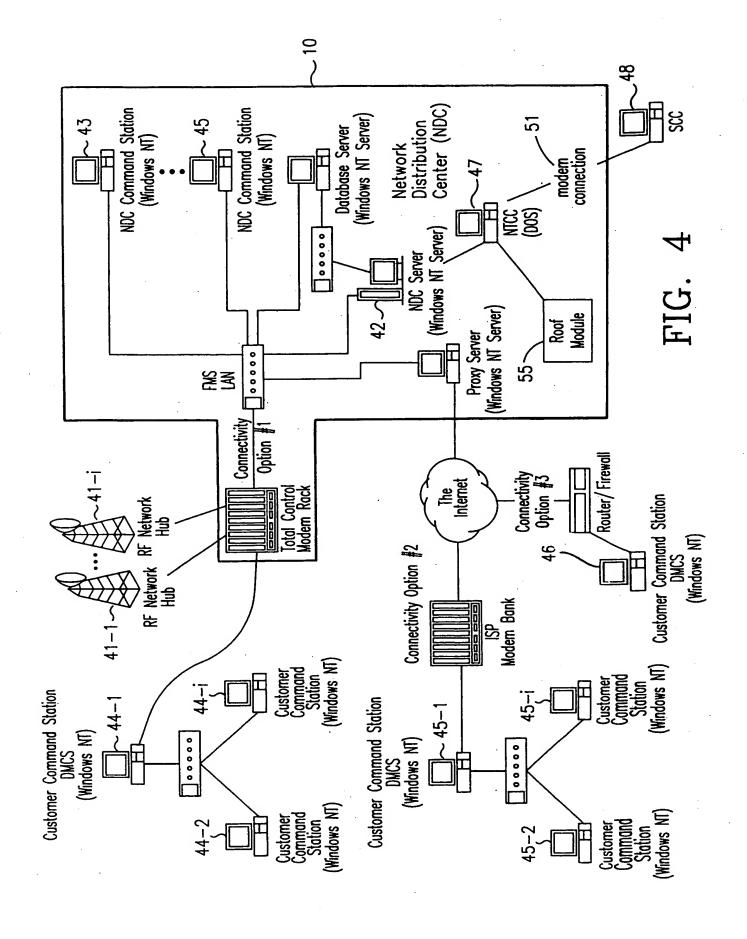
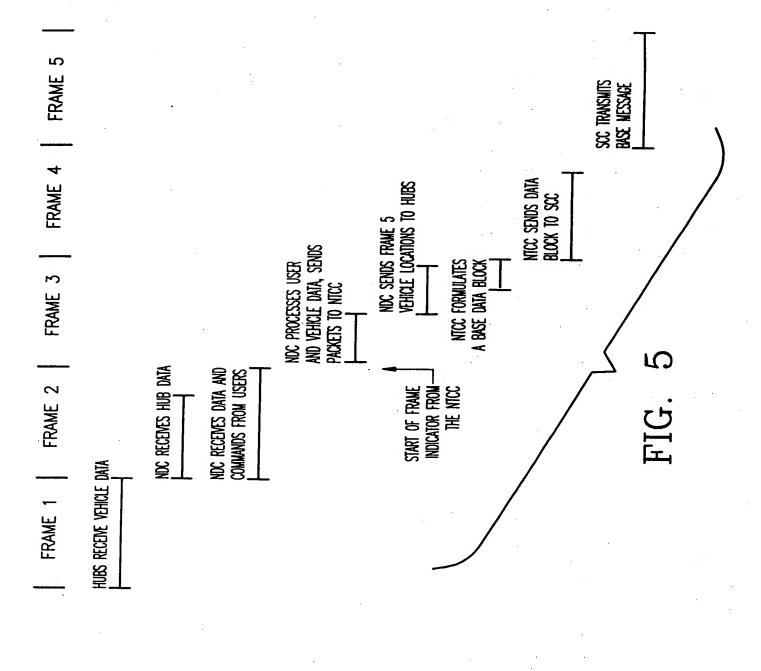
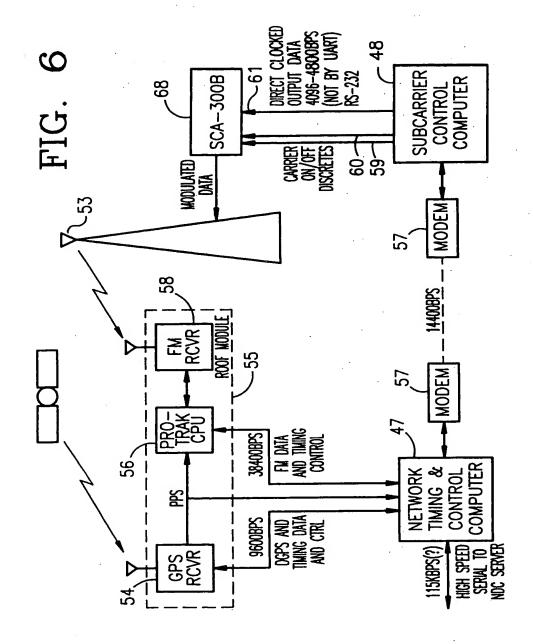


FIG. 2









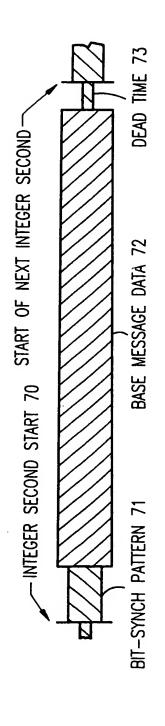
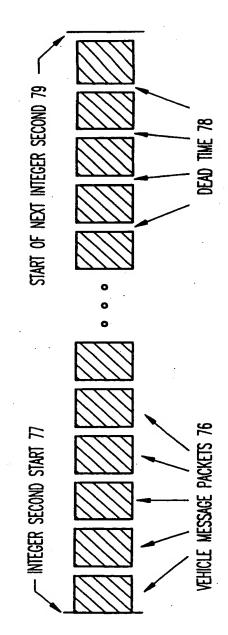
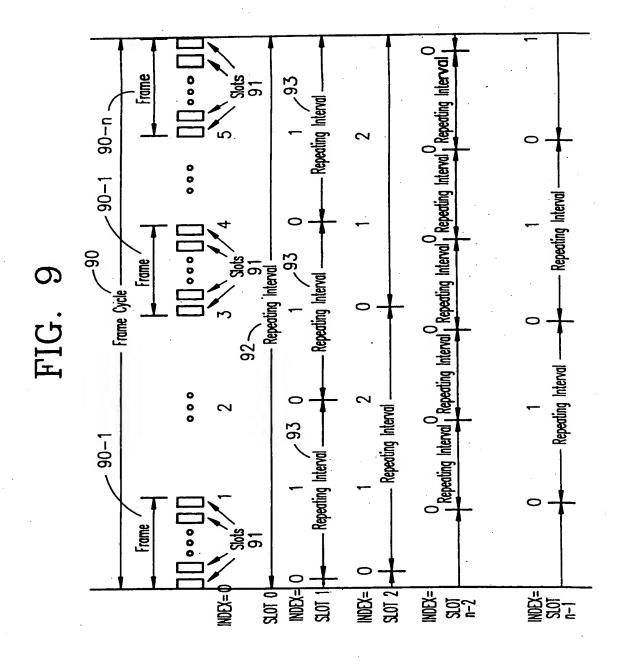


FIG. 7

FIG. 8





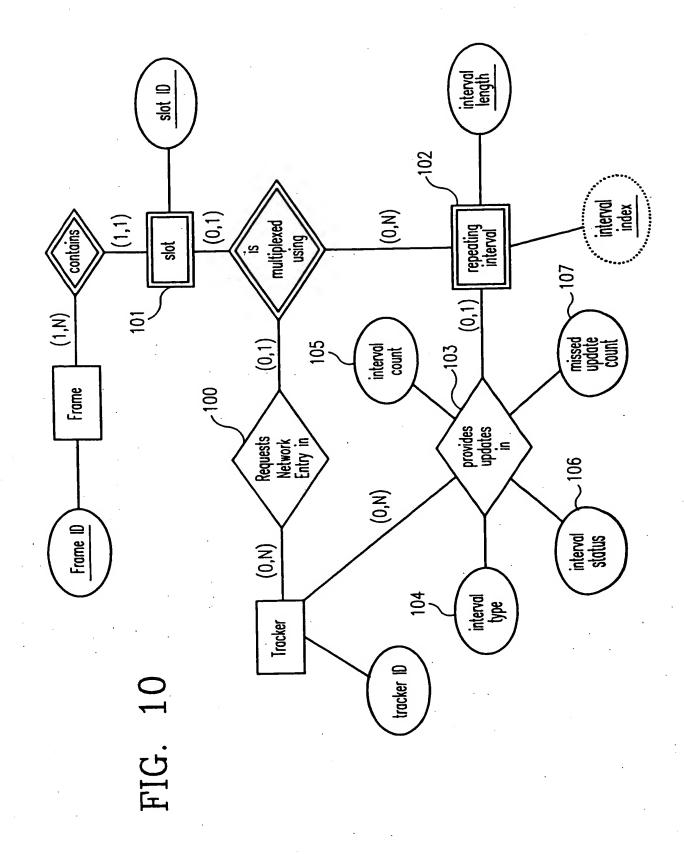
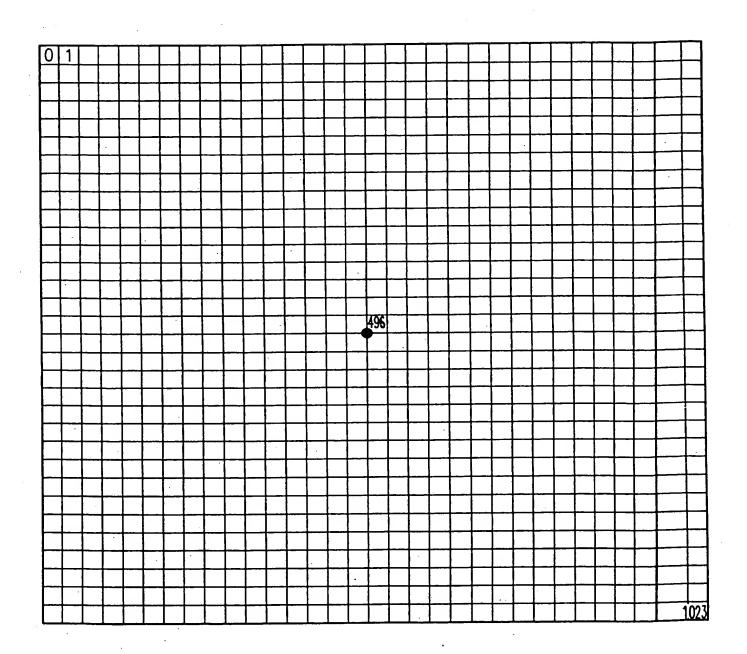


FIG. 11



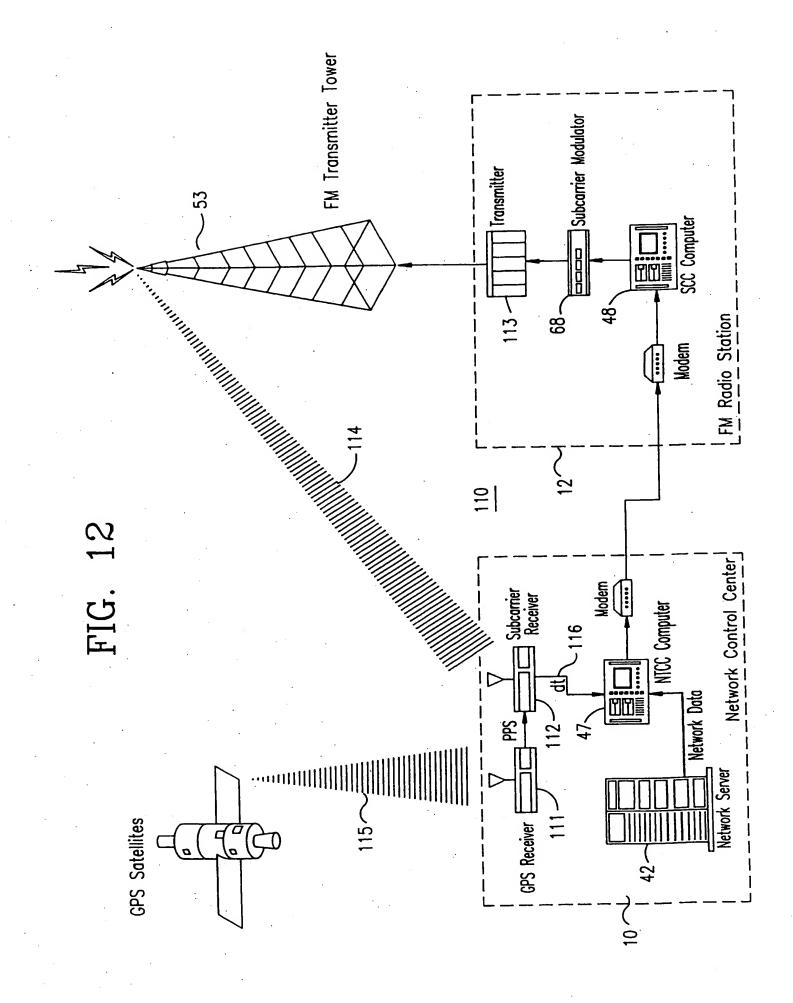


FIG. 13

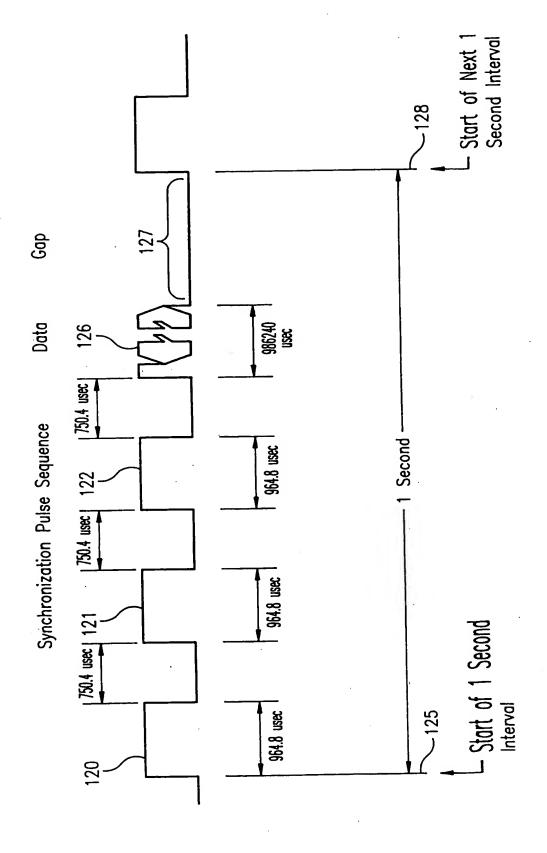


FIG. 14A
Initialization Mode

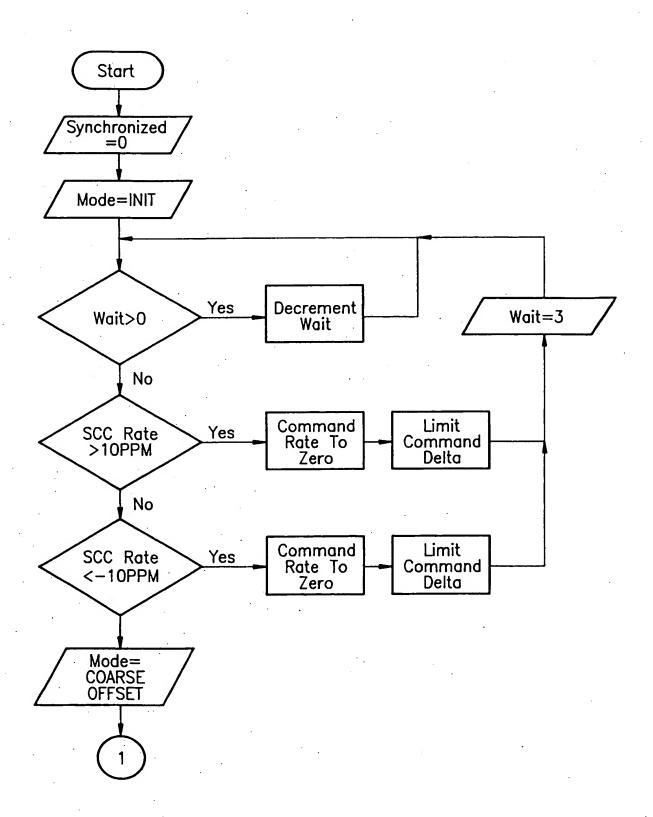
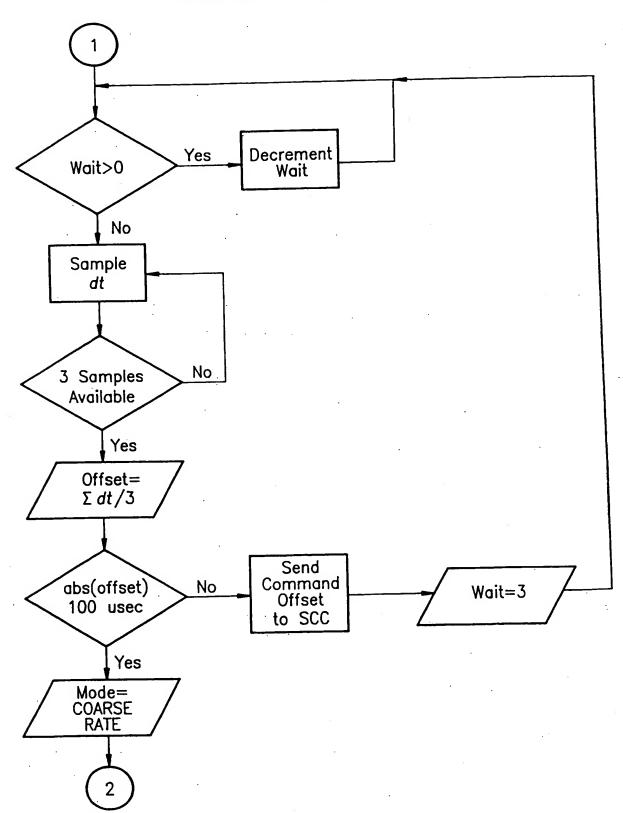
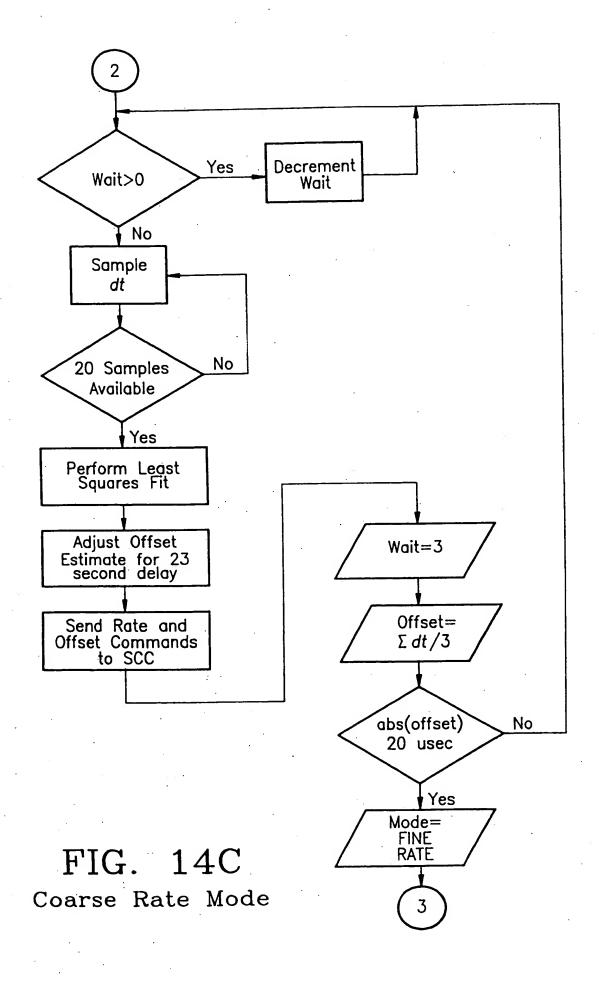
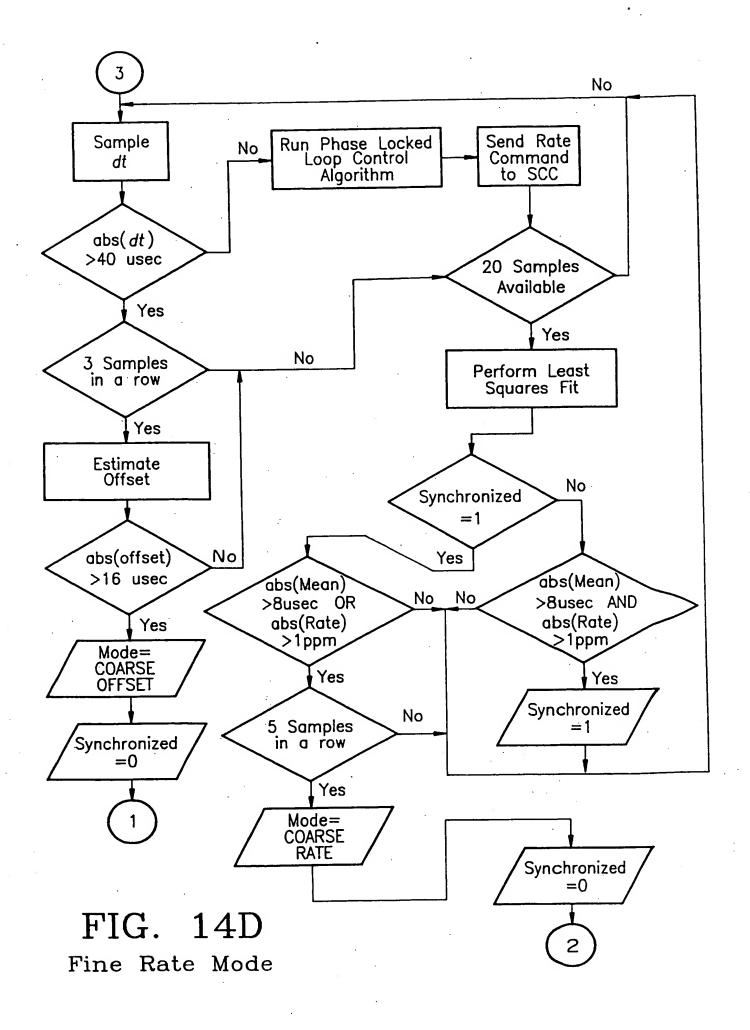


FIG. 14B Coarse Offset Mode







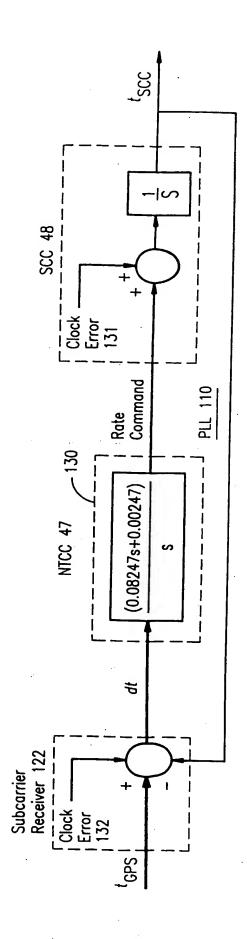
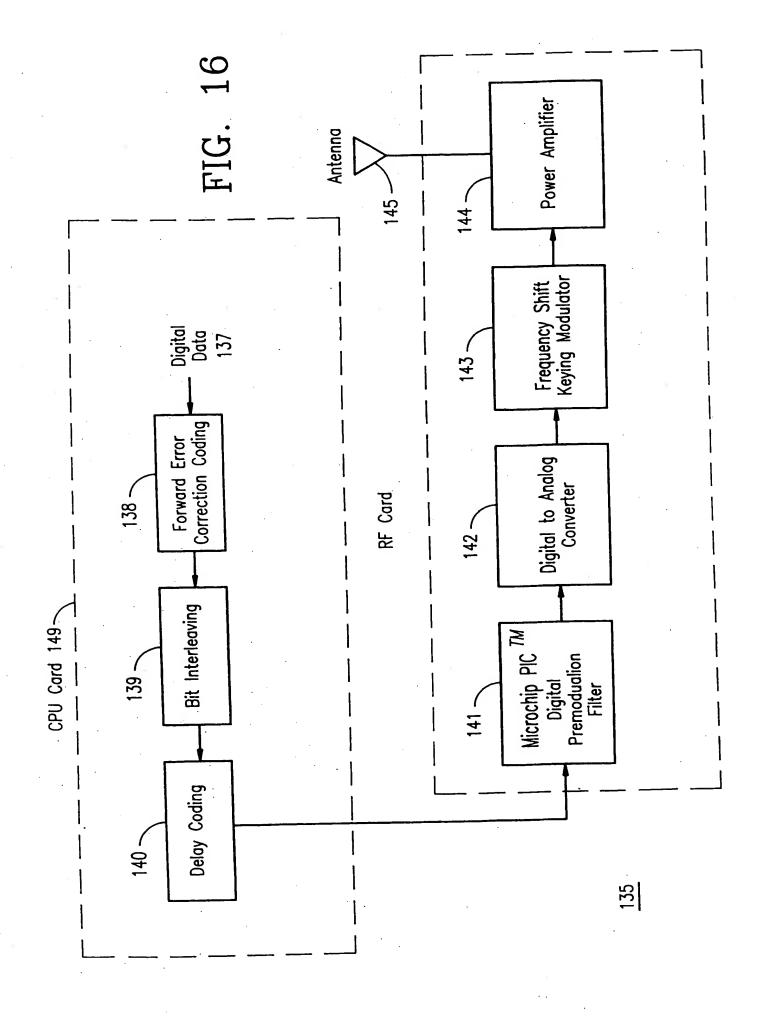
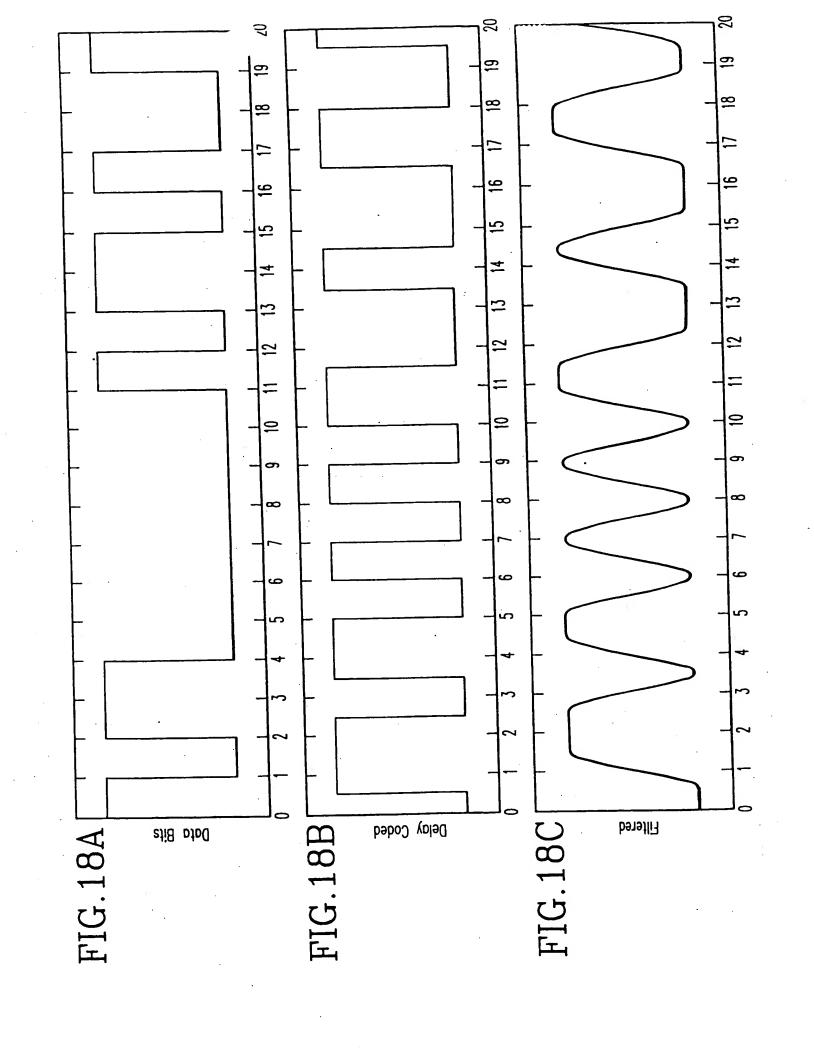


FIG. 15



. 1	011 023 035 047 071 083 083 107 119 119
0	1010 1010 1010 1010 1010 1010
	010 022 030 030 030 030 130 145 145
-	5010 000 000 000 000 000 000 000 000 000
	009 021 033 045 069 069 117 117 117
7	0110/2/2/4/2/2/2/2/2/2/2/2/2/2/2/2/2/2/2/2/
	128 88 88 88 88 88 88 88 88 88 88 88 88 8
m	9/0 10/1 10/1 10/1 10/1 10/1 10/1 10/1 1
4	8/0 007 10/2031 11/3043 0/5 055 1/6 067 2/7 079 3/8 091 6/11127 7/7 139
	006 8 0018 0018 0018 0018 0018 0018 0019 0019
က	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	5
3its 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	6/0 2/10 10/4 11/5 10/4 1/8 1/8 1/8 1/8 1/8 1/8 1/8 1/8 1/8 1/8
7	5/0 004 5/1 016 5/1 016 5/2 028 5/4 05/2 5/6 076 5/6 076 5/6 076 5/7 10 112 1/4 136 indicates
-	1201200220000
eavin 8	0 003 1 015 2 027 3 039 5 063 6 075 6 075 7 087 1 123 1 123 1 123 1 135
Interle	5/40 6/72 10/6
	002 014 014 026 038 038 074 074 074 071 074 074 074 074 074 074 074 074 074 074
DMA Transmit Bit 10 9	54 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5
Trat	001 0025 0037 0037 0037 0049 0049 0049 1121 1121 1131 1131 1131 1131 1131 113
AMOT D1	2/0 3/1,1 5/3/3 10/8 11/9 11/9 1/1 1/1 1/1 1/1 1/1 1/1 1/1 1
	000 012 024 036 048 048 060 072 087 108 1120 132 ds are
=	01084767 0000 € 8000 € 8000 € 8000 € 8000
spool	0-22430-8057

FIG. 17



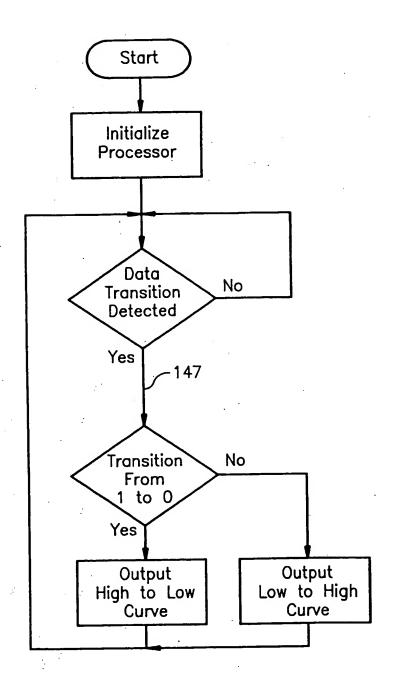
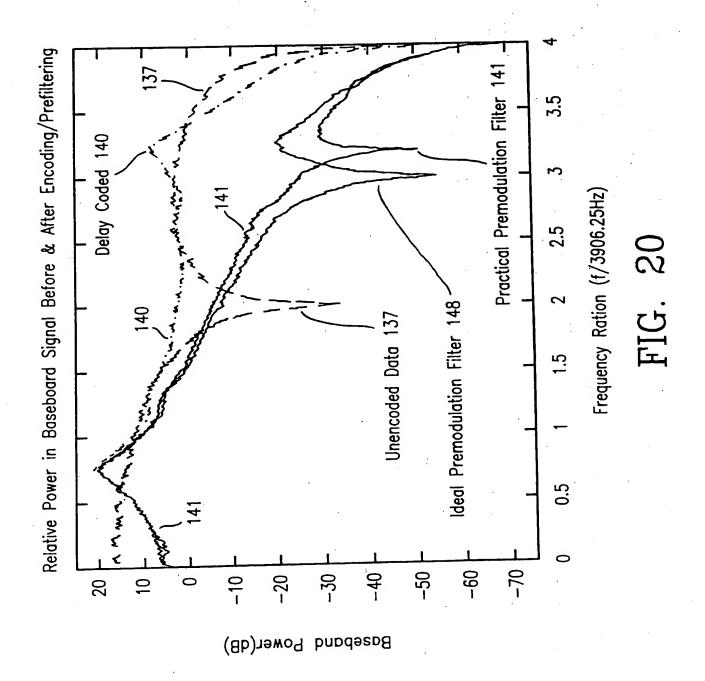
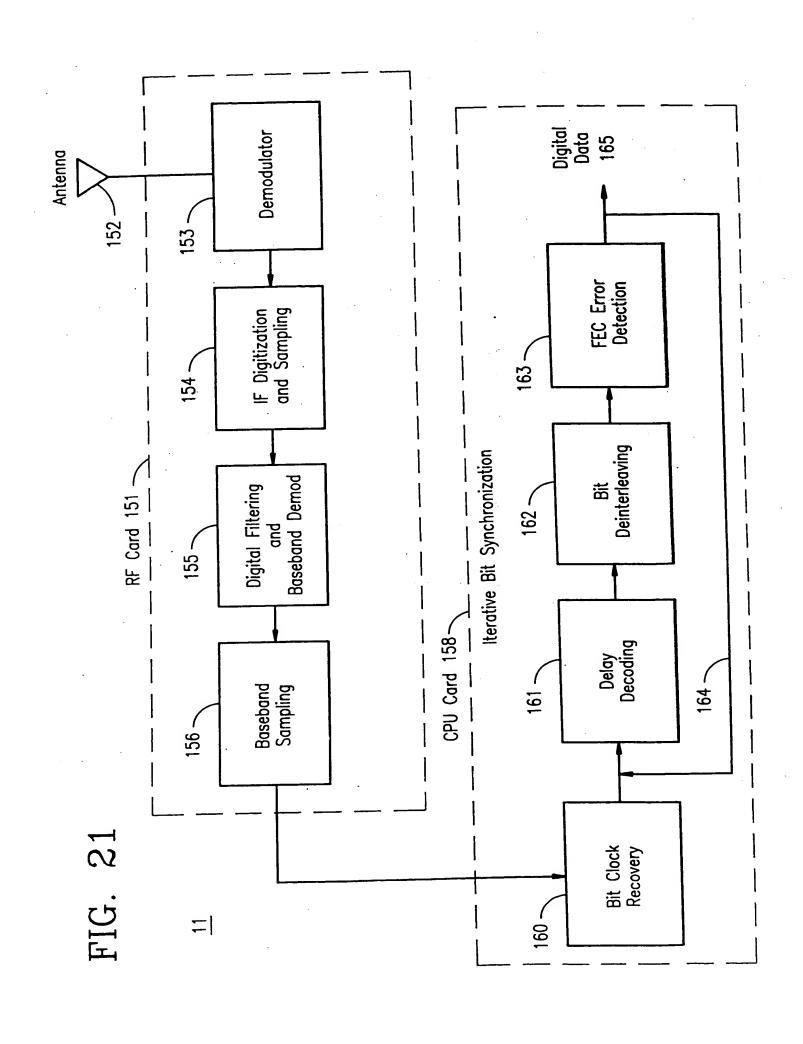
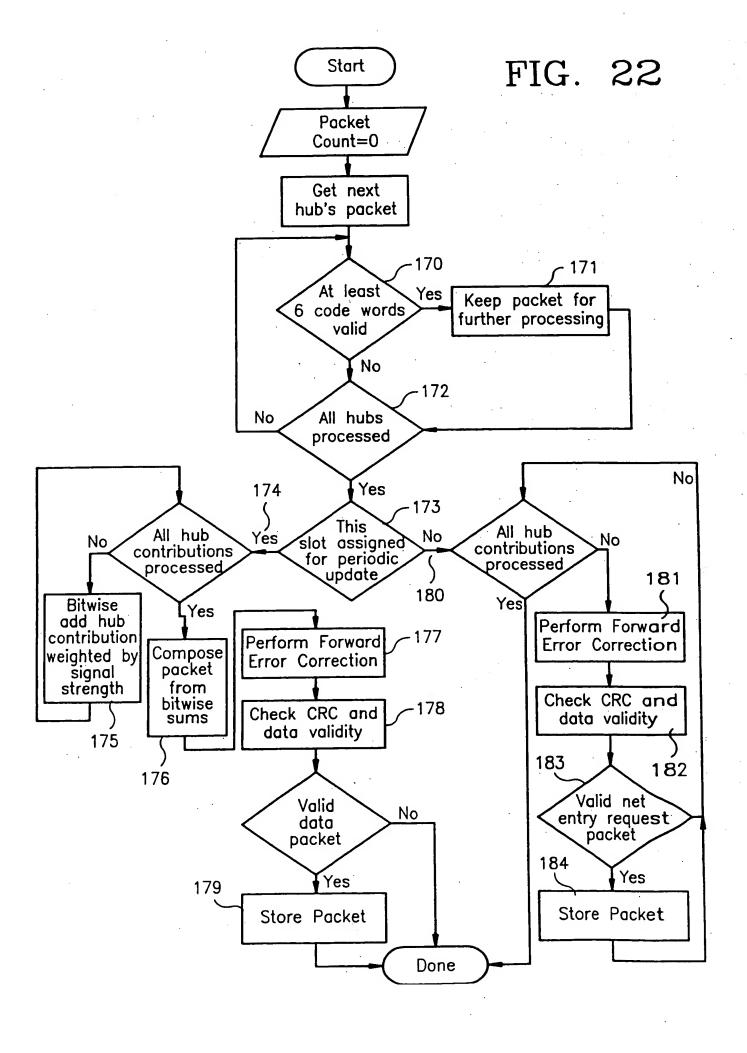
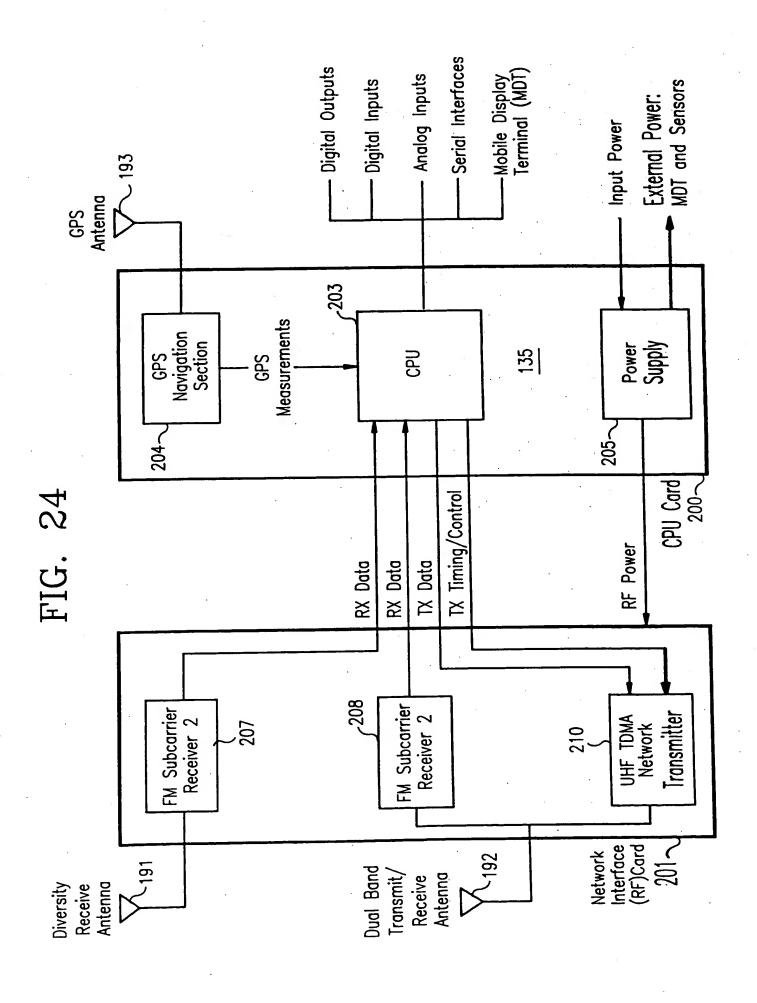


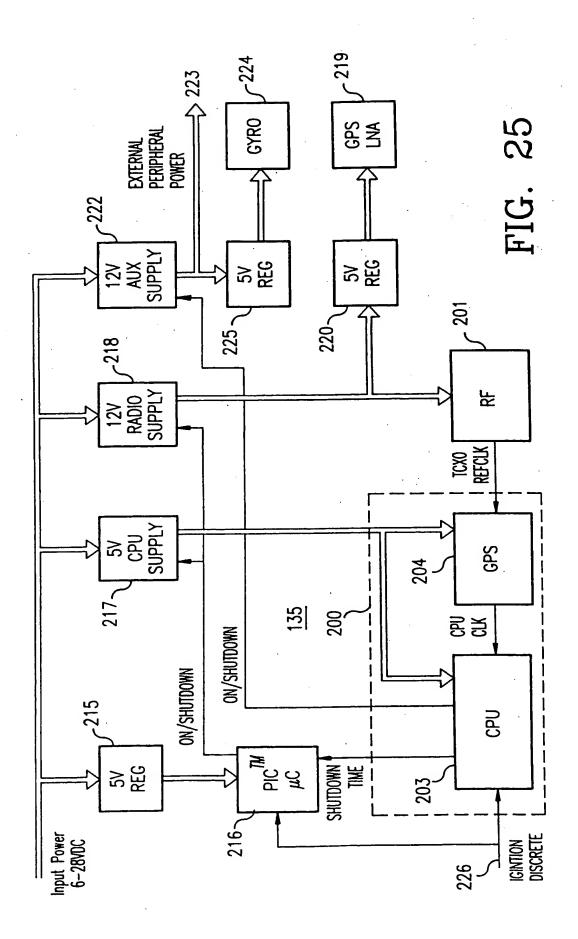
FIG. 19

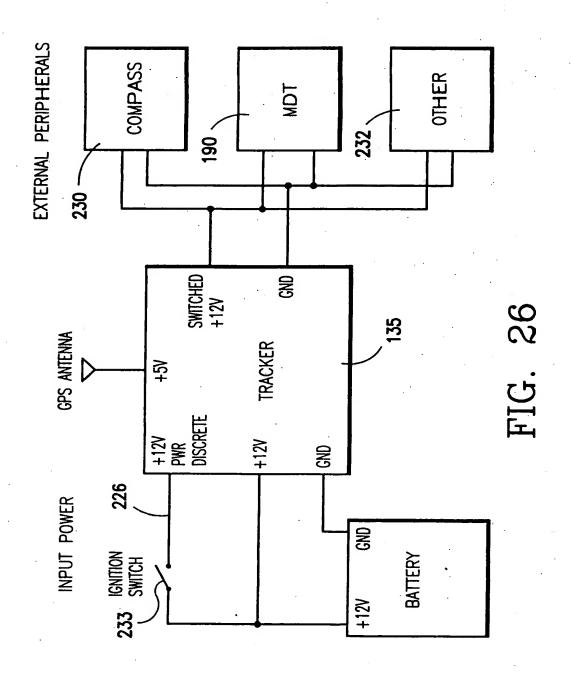


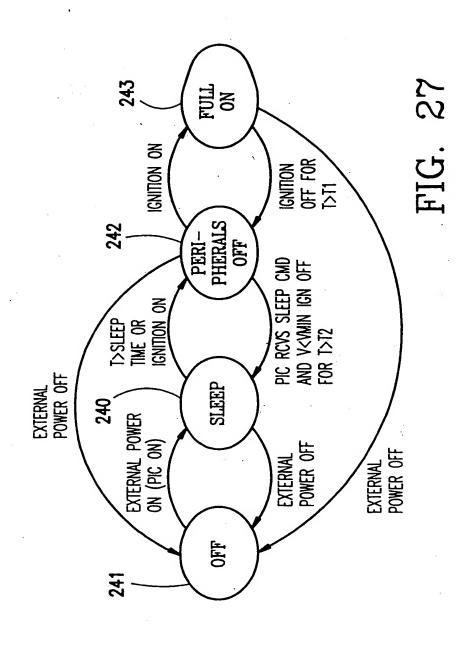












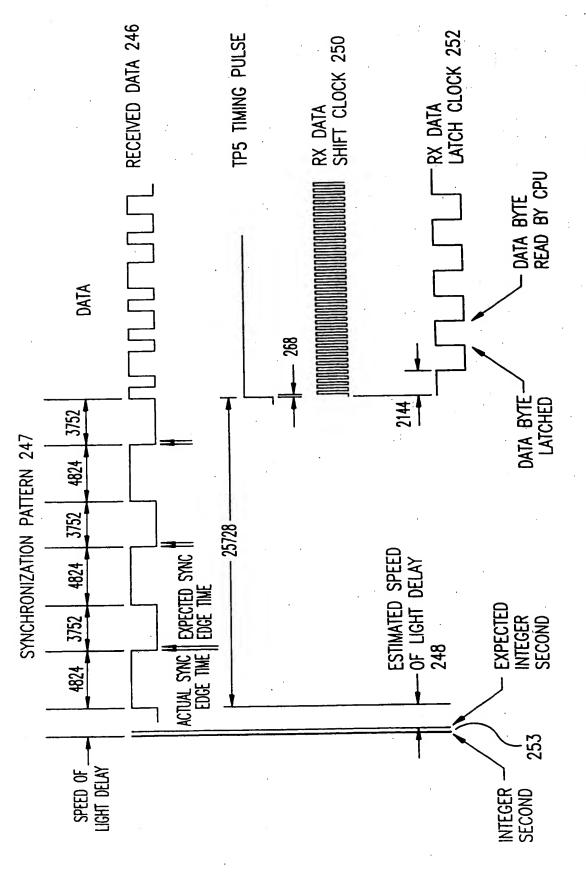


FIG. 28

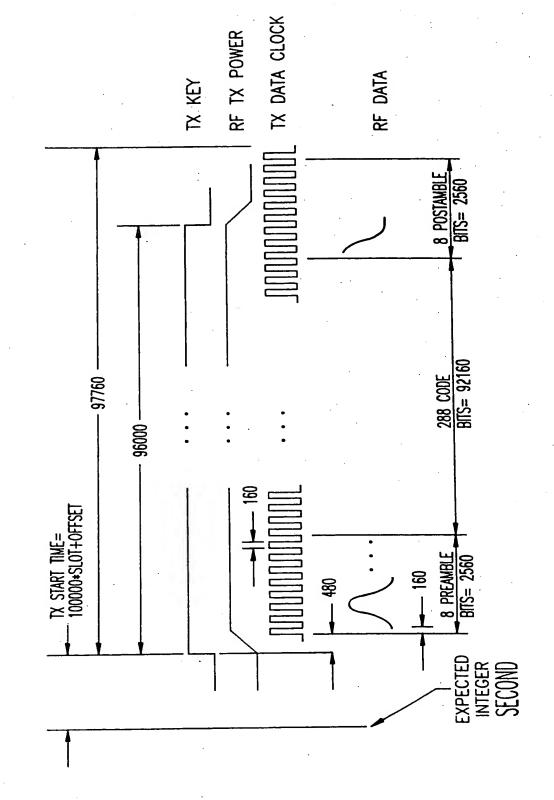
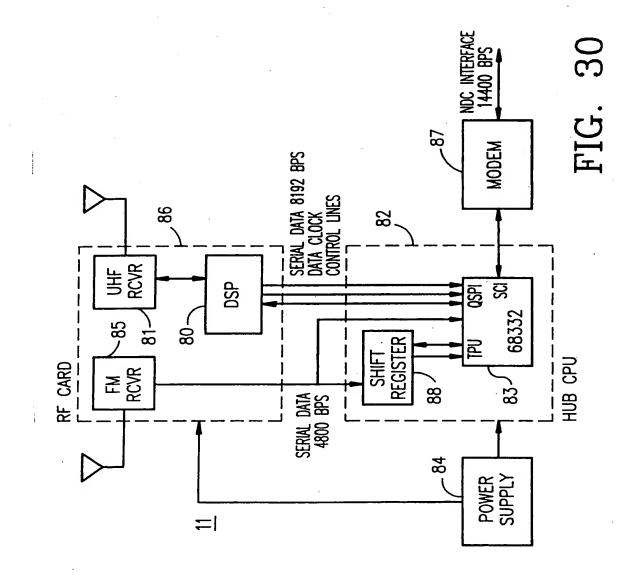
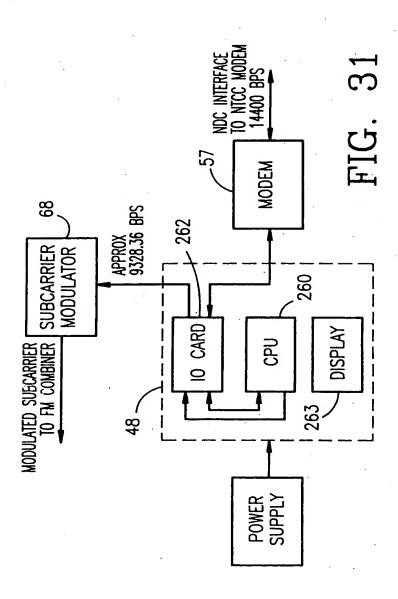
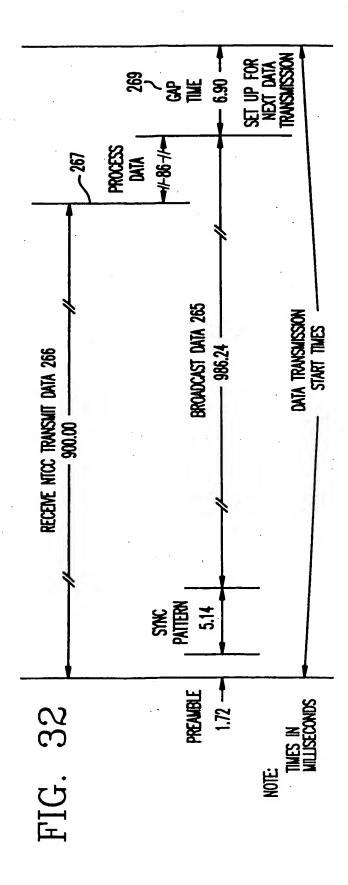


FIG. 29







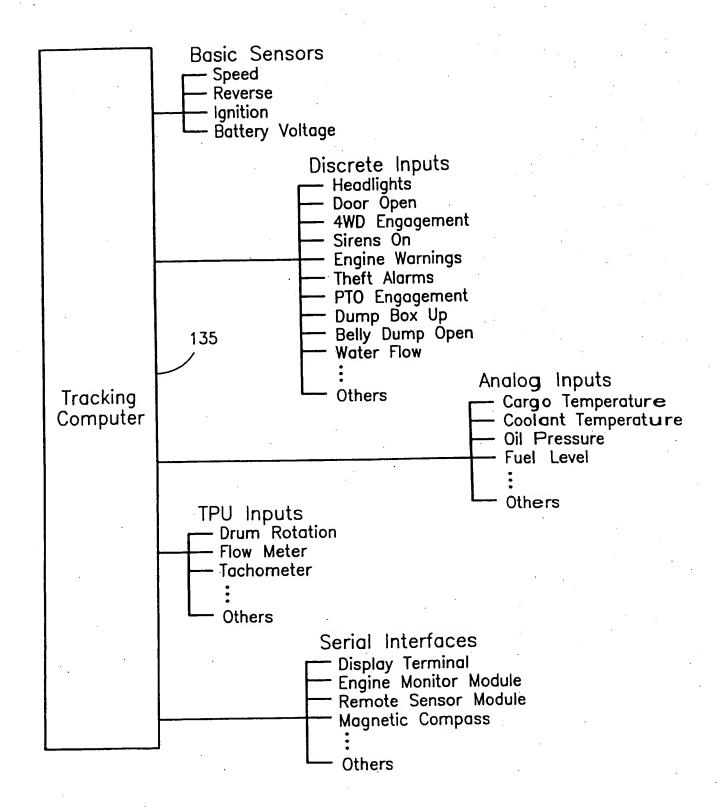


FIG. 33

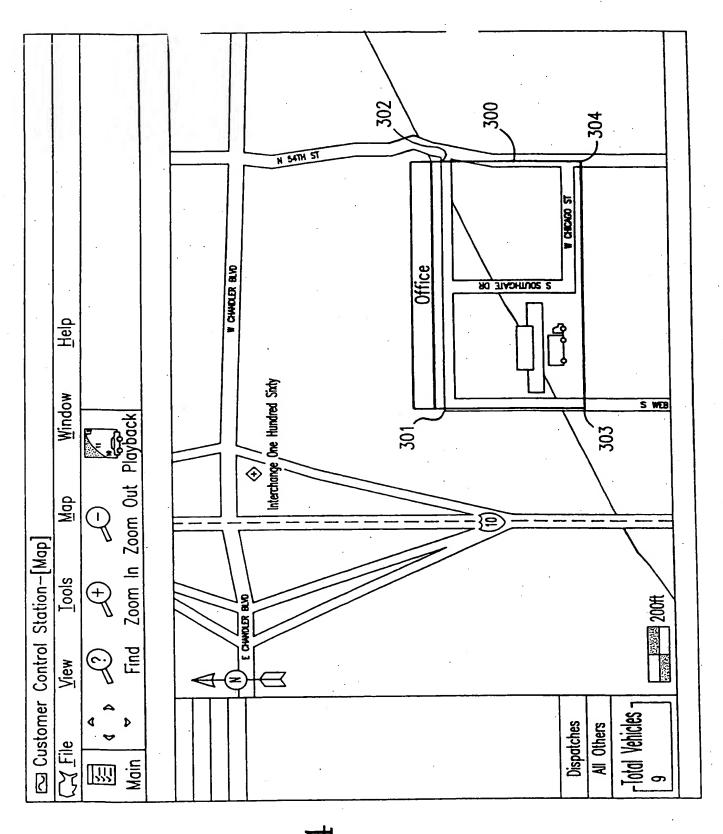


FIG. 34

